#### **REMARKS**

Claims 1-30 are pending in the present application.

This Amendment is in response to the Office Action mailed September 25, 2002. In the Office Action, the Examiner objected to claims 2, 8-9, 12, 18-19, 22, and 28-29, rejected claims 1-5 and 11-15 under 35 U.S.C. §102(b); and claims 6-10 and 16-30 under 35 U.S.C. §103(a). Applicants have amended claims 1, 11, and 21. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

### I. <u>CLAIM OBJECTION</u>

In the Office Action, the Examiner objected to claims 2, 9, 12, 19, 22, and 29. In particular, the Examiner stated that claims 9, 19, and 29 depend upon claims 2, 12, and 22, respectively, which contain alternative language, thus making it unclear whether it was intended for the original claims to definitely include the CAM limitation. Applicants respectfully disagree.

Alternative expressions are permitted if they present no uncertainty or ambiguity with respect to the question of scope or clarity of the claims. MPEP 2173.05(h). A dependent claim depending on a claim with a permissible alternative expression is also permitted. An acceptable form of alternative expression is the Markush claim. MPEP 2173.05(h). If the Examiner objection is sustained, the implication is that a Markush claim cannot have a dependent claim, which is clearly incorrect. Claims 2, 12, and 22 are unambiguous with respect to the question of scope or clarity of the claim because the storage element is either a queue or a CAM.

The Examiner further objected to claims 8, 18, and 28 due to lack of proper antecedent basis for "the comparators". Applicants respectfully disagree. Applicants respectfully direct the Examiner's attention to claims 7, 17, and 27 upon which the respective claims 8, 18, and 28 depend. Claims 7, 17, and 27 recite "a plurality of comparators" which establish the antecedent basis for "the comparators" as recited in the respective claims 8, 18, and 28.

Accordingly, applicants respectfully request the objections to claims 2, 8-9, 12, 18-19, 22, and 28-29 be withdrawn.

## II. REJECTION UNDER 35 U.S.C. §102(B)

In the Office Action, the Examiner rejected claims 1-5 and 11-15 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,996,061 issued to Lopez-Aguado et al. ("Lopez-Aguado"). Applicants respectfully traverse the rejection for the following reasons.

<u>Lopez-Aguado</u> discloses a method for invalidating data identified by software compiler. A prefetch engine adds a stride to the physical address to derive a prefetch address (<u>Lopez-Aguado</u>, Col. 7, lines 18-19). The prefetched addresses are discarded if the derived prefetch address is already stored within the prefetch queue (<u>Lopez-Aguado</u>, Col. 7, lines 66-67; Col. 8, line 1)

<u>Lopez-Aguado</u> does not disclose, either expressly or inherently, a gating circuit to disable an access request to a memory. This aspect of the present invention is supported in the Specification on page 11, lines 6-11, and is recited in amended claims 1, 11, and 21 as follows.

- "... a canceler... to cancel the access request when the access request corresponds to at least P of the stored prefetch, ..., the canceler including a gating circuit to disable the access request to the memory when the access request is canceled." (Amended Claims 1 and 21)
- "... disabling the access request to the memory by a gating circuit when the access request is canceled." (Amended Claim 11)

To anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989).

Therefore, Applicants believe that independent claims 1, 11, and 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejection under 35 U.S.C. §102(b) be withdrawn.

## III. REJECTION UNDER 35 U.S.C. §103(A)

In the Office Action, the Examiner rejected claims 6-10 and 16-30 under 35 U.S.C. §103(a) as being unpatentable over <u>Lopez-Aguado</u> in view of U.S. Patent No. 6,134,633 issued to Jacobs ("<u>Jacobs</u>"). Applicants respectfully traverse the rejection for the following reasons.

<u>Jacobs</u> discloses a prefetch management in cache memory. A prefetch memory supports discarding of prefetch addresses that are associated with operations executed by the processor such as by employing a fully associative prefetch memory when comparing addresses of cache access operations to the addresses held in the prefetch memory (<u>Jacobs</u>, Col. 7, lines 4-10).

<u>Lopez-Aguado</u> and <u>Jacobs</u>, taken alone or in any combination, does not disclose, suggest, or render obvious a gating circuit to disable an access request to a memory when the access request is canceled. There is no motivation to combine <u>Lopez-Aguado</u> and <u>Jacobs</u> because neither of them addresses the problem of gating the access request to disable the access request to a memory. There is no teaching or suggestion that a gating circuit is present. <u>Lopez-Aguado</u> and <u>Jacobs</u>, read as a whole, does not suggest the desirability of gating the access request. Furthermore, <u>Jacobs</u> merely discloses using a fully associative prefetch memory when comparing the addresses of cache access operations, not comparing a prefetch access request.

Therefore, Applicants believe that independent claims 1, 11, and 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §102(b), and 35 U.S.C. §103(a) be withdrawn.

# **VERSION WITH MARKINGS TO SHOW CHANGES MADE**

# IN THE CLAIMS

The following is a set of all amended claims.

1	1. (AMENDED) An apparatus comprising:
2	a storage circuit coupled to a prefetcher to store a plurality of prefetch addresses, the
3	plurality of prefetch addresses corresponding to most recent access requests from a
4	processor, the prefetcher generating an access request to a memory when requested by the
5	processor; and
6	a canceler coupled to the storage circuit and the prefetcher to cancel the access
7	request when the access request corresponds to at least P of the stored prefetch addresses, P
8	being a non-zero integer, the canceler including a gating circuit to disable the access request
9	to the memory when the access request is canceled.
1	11. (AMENDED) A method comprising:
2	storing a plurality of prefetch addresses in a storage circuit, the plurality of prefetch
3	addresses corresponding to most recent access requests from a processor, the prefetcher
4	generating an access request to a memory when requested by the processor; and
5	canceling the access request when the access request corresponds to at least P of the
6	stored prefetch addresses, P being a non-zero integer; and
7	disabling the access request to the memory by a gating circuit when the access request
8	is canceled.
1	21. (AMENDED) A system comprising:
2	a processor to generate prefetch requests;
3	a memory to store data; and
4	a chipset coupled to the processor and the memory, the chipset comprising:
5	a prefetcher to generate an access request to the memory when requested by
6	the processor;
7	a prefetch monitor circuit coupled to the prefetcher, the prefetch monitor
8	circuit comprising:

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9	a storage circuit coupled to the prefetcher to store a plurality of
10	prefetch addresses, the plurality of prefetch addresses corresponding to most
11	recent access requests from the processor; and
12	a canceler coupled to the storage circuit and the prefetcher to cancel
13	the access request when the access request corresponds to at least P of the
14	stored prefetch addresses, P being a non-zero integer, the canceler including a
15	gating circuit to disable the access request to the memory when the access
16	request is canceled.

### **CONCLUSION**

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

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**CERTIFICATE OF MAILING** 

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: \_December 26, 2002

Tu Nguyen